AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): Input buffer ~~type~~ packet switching equipment, comprising:

M input line buffers that store cells inputted from M input lines temporarily in a state that one of said M input line buffers stores cells inputted from corresponding one of said M input lines, in this the M is an integer being 2 or more;

an M × N crossbar ~~type~~ switch, which provides N output lines for switching cells outputted from said M input line buffers based on a cross point on/off control signal, in this N is an integer being 2 or more;

N output line sections, which are provided for each of said N output lines of said M × N crossbar ~~type~~ switch, for outputting cells applied switching at said M × N crossbar ~~type~~ switch to N external output lines; and

an arbiter that outputs a connection permission signal to one of said M input line buffers based on connection request signals outputted from said M input line buffers, and also outputs said cross point on/off control signal to said M × N crossbar ~~type~~ switch, and outputs said connection permission signal at a designated slower timing interval than a normal timing interval to one input line buffer that outputs cells to an external output line whose output line rate is slower than a corresponding input line rate,

wherein said designated slower timing interval is a constant periodic rate which is slower than said corresponding input line rate, said designated slower timing interval is set so that arrival of cells at said output line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented.

2 (currently amended): Input buffer ~~type~~ packet switching equipment accordance with claim 1, wherein:

said arbiter, comprising:

a connection request signal processing section that receives said connection request signals from said M input line buffers and processes said received connection request signals;

a contention controller for deciding that one of said M input line buffers requested the connection reads cells for what external output line based on the connection request from said M input line buffers outputted from said connection request signal processing section; and

a connection permission signal processing section that outputs said connection permission signal to one of said M input line buffers based on the contention processed result from said contention controller and also outputs said cross point on/off control signal to said M × N crossbar ~~type~~ switch, and wherein:

in case that said connection permission is given to one input line buffer which outputs cells to the external output line whose output line rate is slower than the corresponding input line rate, said connection permission signal processing section controls so that said contention

controller does not execute the contention control for a designated interval corresponding to the slower output line rate than the input line rate.

3. (currently amended): Input buffer ~~type~~ packet switching equipment in accordance with claim 2, wherein:

in case that said connection permission is given to one input line buffer which output cells to the external output line whose output line rate is slower than the corresponding input line rate said connection permission signal processing section outputs a mask signal for stopping the contention control for a designated period to said contention controller and also outputs a mask cancellation signal for canceling the stopping of said contention control after passing said designated period to said contention controller.

4. (currently amended): Input buffer ~~type~~ packet switching equipment in accordance with claim 3, wherein:

said designated period is designated times of a normal timing interval of said connection permission signal in the case that said connection permission is given to one input line buffer for an external output line whose output line rate is the same that the corresponding input line has.

5 (currently amended): Input buffer ~~type~~ packet switching equipment in accordance with claim 1, wherein:

each of said M input line buffers comprising:

N FIFOs, whose number is the same that said output lines of said M × N crossbar ~~type~~ switch have, for storing cells for said N external output lines temporarily and outputting said connection request signal at the time when said cells are stored;

a distributor that distributes cells inputted from said M input lines to each of said FIFOs, corresponding to said external output line obtained from header information of said cells; and a selector that selects one FIFO to be read corresponding to said connection permission signal inputted from said arbiter from said N FIFOs.

6. (currently amended): An input buffer ~~type~~ packet switching equipment in which an output line rate is converted, the input buffer ~~type~~ packet switching equipment comprising:

M input line buffers that store cells inputted from M input lines temporarily in a state that one of said M input line buffers stores cells inputted from corresponding one of said M input lines, in this the M is an integer being 2 or more;

an M × N crossbar ~~type~~ switch, which provides N output lines for switching cells outputted from said M input line buffers based on a cross point on/off control signal, in this N is an integer being 2 or more;

N output line sections, which are provided for each of said N output lines of said M × N crossbar ~~type~~ switch, for outputting cells applied switching at said M × N crossbar ~~type~~ switch to N external output lines; and

an arbiter that outputs a connection permission signal to one of said M input line buffers based on connection request signals outputted from said M input line buffers, and also outputs

said cross point on/off control signal to said M × N crossbar ~~type~~ switch, wherein said arbiter, outputs said connection permission signal to one of said M input line buffers by using a designated slower timing interval than a normal timing interval in case that cells are outputted to an external output line whose output line rate is slower than a corresponding input line rate, and

wherein said designated slower timing interval is a constant periodic rate which is slower than said corresponding input line rate, said designated slower timing interval is set so that arrival of cells at said output line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented.

7. (previously presented): A method of outputting data in packet switching, comprising:

storing data inputted from a plurality of input lines; and

selectively outputting said stored data to a plurality of external line sections;

wherein said stored data output to an external line section with an output line rate slower than a corresponding input line rate is outputted at a designated rate slower than said corresponding input line rate, and

wherein said designated slower rate is a constant periodic rate which is slower than said corresponding input line rate, said designated slower rate is set so that arrival of said outputted stored data at said external line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented.

8. (previously presented): The method of claim 7, wherein said designated rate corresponds to said output line rate.

9. (previously presented): The method of claim 7, wherein said stored data is outputted to said plurality of external line sections at rates corresponding to respective input line rates when output line rates of said plurality of external line sections are at least the corresponding input line rates.

10. (previously presented): The method of claim 7, wherein said external line section is a bufferless component.